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SYSTEM FOR CONVERTING HARDWARE DESIGNS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO HARDWARE IMPLEMENTATIONS

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Cross-Reference to Microfiche Appendix

Appendix A, which is a part of the disclosure in parent U.S. Patent Application Serial No. 08/931,148 filed on September 16, 1997 and which is incorporated herein in its entirety by this reference, is a microfiche appendix consisting of two sheets of microfiche having a total of 176 frames. Microfiche Appendix A is a source code listing of a portion of the code comprising one embodiment of a system for converting hardware designs in a high-level programming language (ANSI C) into a register transfer level hardware description language (Verilog), which is described in more detail below.

Field of the Invention

This invention relates to configuring digital circuits, especially computationally intensive digital circuitry, such as field programmable gate arrays (FPGAs) and other programmable logic hardware and application specific integrated circuits (ASICs), and, more particularly, to computer aided design of such computationally intensive digital circuitry. Specifically, one embodiment of the invention provides a system for converting